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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/211,718	12/14/1998	ERIC R. FOSSUM	08305/015001	9540

7590 09/26/2003

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EXAMINER	
GENCO, BRIAN C	
ART UNIT	PAPER NUMBER
2615	18

DATE MAILED: 09/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/211,718	FOSSUM ET AL.	
	Examiner	Art Unit	
	Brian C Genco	2615	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Applicant's amendment filed July 29, 2003 has been fully considered by the Examiner but is not deemed persuasive.

Applicant argues that Heller cannot be considered prior art due to the claim to domestic priority of provisional application number 60/069,700 filed December 16, 1997.

In response Examiner notes the previous office action wherein it was detailed that the provisional application does not provide adequate support under 35 U.S.C. 112 for claims 1-12 since there is no teaching of a pixel interpolator located between the image area and the fourth edge. Examiner included a copy of Applicant's provision application, wherein on lines 13-14 Applicant discloses that pixel interpolation be done in software and further on lines 19-22 that Applicant discloses an on-chip timing and control system, however this does not enable on-chip pixel interpolation. Examiner again asserts that due to the failure of provisional application number 60/069,700 filed December 16, 1997 to teach on-chip pixel interpolation no priority is granted to those claims claiming on-chip pixel interpolation. As such previously presented claims 1-12 are not subject to the claim for domestic priority and further newly presented claims 14, 17, and 18 are also not subject to the claim for domestic priority. Examiner notes that claim 16 is broad enough to cover providing off-chip software interpolation and as such has benefit of Applicant's claim to priority. Further, newly added claims 13 and 15 do not claim interpolation and as such have benefit of Applicant's claim to priority. As such Heller is valid prior art for claims 1-12, 14, 17, and 18.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on

combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

In response to applicant's arguments that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Examiner notes the previous office action wherein all of the motivation to combine was found in the references themselves.

Applicant argues that Spivey does not disclose "row logic being physically located inside said image sensor in place of a plurality of pixels of the array forming said image sensor".

In response, Examiner disagrees. Examiner notes that Spivey specifically teaches that in an alternative embodiment "for combining arrays involves fabrication of a four-sided buttable array with the readout circuitry integrated with the pixel array (column 26, lines 36-38)." Examiner notes that readout circuitry includes row logic and further that since the readout circuitry is integrated with the pixel that means that the readout circuitry must physically be located inside the image sensor as describe in column 26, lines 33-52.

Applicant argues that Spivey teaches away from the use of a pixel interpolator by treating the pixel locations taken by the wire bond connections as dead pixels.

In response, Examiner notes that this is not teaching away. In fact, in combination with Heller this teaches that these "dead pixel" locations are in need to be interpolated.

Applicant argues that Sayag teaches away from the idea of butting a plurality of image sensors with the description of chamfered corners.

In response, Examiner notes again that this is not teaching away. Examiner notes the previous office action wherein the Sayag reference was used as a way to illustrate a possible way of providing readout circuitry integrated with the pixel array as taught by Spivey. Further, upon reconsideration of the Sayag reference Examiner notes that Sayag teaches that the image sensors could be made as octagons with each edge equal in length (column 4, lines 40-43). As such one would be able to but the image sensors, if necessary, without substantial loss in the corners as argued by Applicant in previous responses.

Applicant argues that Sayag teaches away from pixel interpolation since Sayag teaches to multiply image signals of the partially optically active readout circuits by a constant.

In response, Examiner notes column 7, lines 4-8 of Sayag wherein it is taught to multiply the signals of the central read-out register by a constant **so as to match the other pixels** (emphasis added). Examiner notes that Merriam-Webster's Collegiate Dictionary defines interpolate as: "to estimate values of (a function) between two known values". Examiner notes that since the constant is used to match the other pixels then the other pixels, or known values, are used to estimate the values of the signals of the central read-out register. As such Sayag does perform pixel interpolation.

Applicant argues that Thevenin teaches away from pixel interpolation.

In response, Examiner notes that Thevenin specifically teaches to perform pixel interpolation in column 11, lines 17-29, and in particular line 29.

Applicant argues that Thevenin does not teach buttable image sensors.

In response, Examiner notes that that teaching is not needed in the disclosure of Thevenin, however, Examiner does note that Thevenin does specifically teach butting image sensors as shown in Fig. 8 and described in column 10, line 61 – column 11, line 16.

For all of the above reasons Applicants amendment has not been deemed persuasive.

Examiner's Notes

The official notice presented in the previous action stating that it is very well known and established in the art that CCD and CMOS image sensors are analogous art and that CMOS image sensors are preferable since they cost less to manufacture was not traversed and is accordingly taken as an admission of the fact noted.

The official notice presented in the previous action stating that it is it is very well known and established in the art to make the spaces between the edge of the image sensor and the edge of the chip as small as possible so as to increase image sensitivity when butting image sensors was not traversed and is accordingly taken as an admission of the fact noted.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 1 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "sensor[[s]]" in the third paragraph of claim 1. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claims 1-12, 14, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 5,886,353 to Spivey et al) in view of (USPN 5,510,623 to Sayag et al) in further view of (USPN 5,937,027 to Thevenin et al) in still further view of (USPN 6,396,539 to Heller et al) in still further view of (Applicant's admitted prior art).

In regards to claim 1 Spivey et al, herein Spivey, discloses a CMOS image sensor circuit, comprising:

a first CMOS image sensor substrate, said substrate having an image sensor portion arranged in an array of pixels of rows and columns, and image sensor logic on said substrate, said image sensor logic being electrically connected to said image sensor portion, said image sensor logic including row logic associated with each of said rows individually, and chip logic associated with parts of said image sensor portion other than rows individually, said image sensor portion having a first portion and a second portion (e.g., column 4, line 57 – column 5, line 1; Fig. 15A; column 11, line 63 – column 12, line 5; column 12, lines 50-52; note that the chip logic associated with parts of said image sensor other than rows individually is readout circuit 133; as noted below when combined with Thevenin and Sayag the image sensor is divided into two portions since the readout circuit is located through the center of the image sensor),

said image sensor substrate formed to have at least a first set of parallel edges including a first edge and a second edge, and a second set of parallel edges, different than said first set of parallel edges, and second set of parallel edges including a third edge and a fourth edge (e.g., Fig. 15A),

said image sensor substrate extending between said first edge, said second edge, and said third edge, such that said first portion of said image sensor portion is adjacent said first edge and said third edge of said image sensor substrate and said second portion of said image sensor portion is adjacent said second edge and said third edge of said image sensor[[s]] substrate (e.g., column 26, lines 33-52; note that if the readout circuitry is integrated with the pixel array then there would be image sensors adjacent the first, second, and third edges; note Examiners comments on the combination of Sayag and Thevenin to Spivey as discussed both above and below),

said row logic being physically located inside said image sensor (e.g., column 26, lines 33-52)

chip driver circuitry located between said first portion and said second portions of said image sensor portion and said fourth edge of said image sensor substrate (e.g., Fig. 15A); and

a second CMOS image sensor substrate configured similarly to said first CMOS image sensor substrate and abutted to one of said edges of said first CMOS image sensor substrate (e.g., Figs. 17A, 19, and 20A)

Spivey does not disclose that said row logic be in place of a plurality of pixels of the array or a pixel interpolator between said first portion and said second portions of said image sensor portion and said fourth edge of said image sensor substrate.

It is known in the art to place row logic inside said image sensor in place of a plurality of pixels as taught by Thevenin et al, herein Thevenin, and Sayag et al, herein Sayag. Thevenin discloses an invention for monitoring the exposure so as to maximize the image quality and minimize the dose of x-rays to an object of an x-ray imager by using two two-pixel-wide

measurement areas (e.g., Fig. 3B; column 6, lines 42-61; column 7, lines 12-21; column 8, lines 21-27). Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have used exposure monitoring in the x-ray imager of Spivey in order to optimize "exposure time of the object to ... radiation so as to produce at each taking of an image, an image of good quality while minimizing the dose of radiation to which the object is subjected (column 1, lines 9-12, Thevenin)." Sayag discloses the use of a centrally disposed read-out register that is photosensitive in order to monitor exposure (column 6, lines 57 – column 7, line 8; column 7, lines 29-32). This would be a preferred method of monitoring exposure since only one two-pixel-wide measuring area would be used and thus less correction of missing pixels would be needed. Further, this would be preferred since the readout circuits are photosensitive one would gain the benefit of both exposure monitoring as taught by Thevenin and having the readout circuit in the interior of the image sensor so as to enable better butting of image sensors so as to form a large format array. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have had a centrally disposed photosensitive readout register so as to monitor x-ray exposure in order to maximize image quality while minimizing radiation dose as well as enabling butting of multiple arrays so as to form a large format array.

Assuming arguendo for combining the Sayag reference since the Sayag reference deals with a CCD image sensor an the other references deal with CMOS image sensors, Examiner notes that based on Applicants admission of fact, it is very well known and established in the art that CCD and CMOS image sensors are analogous art and that CMOS image sensors are preferable since they cost less to manufacture. Therefore it would have been obvious to one of

ordinary skill in the art at the time of the invention to have made Sayag's invention using CMOS image sensor technologies in order to reduce cost.

It is also known in the art to use on-chip pixel interpolation as taught by Heller et al, herein Heller. Heller discloses having an on-chip memory and controller unit for storing defective pixel locations so that the controller can interpolate values for the defective pixels from the surrounding pixels (e.g., column 8, lines 39-65; column 4, lines 5-9). Note that Heller discloses that it is preferable to include as much circuitry on-chip in order to reduce cost (column 1, line 56 – column 2, line 36). While Spivey and Thevenin both disclose using pixel interpolation this process is done off-chip, therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have preformed pixel interpolation on-chip in order to reduce cost. Furthermore it would have been obvious to one of ordinary skill in the art at the time of the invention to have place the pixel interpolator between said image area and said fourth edge so as to still enable butting for the creation of a large format array as taught by Spivey.

In regards to claim 2 Sayag discloses an embodiment in column 6, lines 6-15 wherein the "row logic is formed in place of two columns of the array."

In regards to claim 3 Spivey discloses that the image sensor has a thin edge around three of the sides, however this edge is about 4 pixel pitches wide (column 11, line 61 – column 12, line 5). Examiner notes that based on Applicants admission of fact it is very well known and established in the art to make these edges as small as possible so as to increase image sensitivity when butting image sensors. Therefore it would have been obvious to one of ordinary skill in the

art at the time of the invention to have made the edge on Spivey's image sensor to come within 2 pixel pitches instead of 4 in order to increase sensitivity of a large format array.

In regards to claim 4 see Examiners notes on the rejection of claim 1.

In regards to claim 5 see Examiners notes on the rejection of claim 1.

In regards to claim 6 see Examiners notes on the rejection of claim 1.

In regards to claim 7 see Examiners notes on the rejection of claim 3. Note that the edge around Spivey's image sensor is a guard ring.

In regards to claim 8 see Examiners notes on the rejection of claims 1 and 3.

In regards to claims 9-12 see Examiners notes on the rejection of claim 1.

In regards to claim 14 and 17 see Examiners notes on the rejection of claim 1.

In regards to claim 18 see Examiners notes on the rejection of claim 1. Note that the claimed limitation of integrating the control portions of said at least two CMOS image sensors in inherent with providing a large format image sensor as disclosed by Spivey.

Claims 13, 15, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over (USPN 5,886,353 to Spivey et al) in view of (USPN 5,510,623 to Sayag et al) in further view of (USPN 5,937,027 to Thevenin et al).

In regards to claims 13 and 15 see Examiners notes on the rejection of claim 1. Since claims 13 and 15 gain benefit of Applicants provisional application disregard the teaching and combination of the Heller reference noted above in the rejection of claim 1 in consideration with claims 13 and 15.

In regards to claim 16 see Examiners notes on the rejection of claim 15. Note that it is very well known and established in the art to perform interpolation for missing pixels and further for spaces between image sensor chips when butting arrays of image sensors in order to reduce image losses caused by missing pixels and spaces formed between butted image sensors. Official notice is taken. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to have preformed pixel interpolation in order to reduce image losses caused by missing pixels and spaces formed between butted image sensors.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian C. Genco who can be reached by phone at 703-305-7881 or

by fax at 703-746-8325. The examiner can normally be reached on Monday thru Friday 8:00am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrew Christensen can be reached on 703-308-9644. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the technology center 2600 customer service office whose telephone number is 703-306-0377.

Brian C Genco
Examiner
Art Unit 2615

August 29, 2003

ANDREW CHRISTENSEN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600